THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

ARBOR GLOBAL STRATEGIES LLC,	§	
	§	
Plaintiff,	§	
	§	
v.	§	Case No. 2:19-cv-00333-JRG
	§	
SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., and SAMSUNG SEMICONDUCTOR, INC.,	§	
	§	
Defendants.	§	

CLAIM CONSTRUCTION
MEMORANDUM AND ORDER

On November 10, 2020, the Court held a hearing to determine the proper construction of disputed terms in United States Patents No. 6,781,226, 7,282,951, and RE42,035. Before the Court is the Opening Claim Construction Brief (Dkt. No. 79) filed by Plaintiff Arbor Global Strategies LLC ("Plaintiff" or "Arbor"). Also before the Court is the Responsive Claim Construction Brief (Dkt. No. 91) filed by Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively, "Defendants" or "Samsung") as well as Plaintiff's reply (Dkt. No. 97). Having reviewed the arguments made by the parties at the hearing and in their claim construction briefing, having considered the intrinsic evidence, and having made subsidiary factual findings about the extrinsic evidence, the Court hereby issues this Claim Construction Memorandum and Order. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc); *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015).

Table of Contents

I. BACKGROUND

Plaintiff alleges infringement of United States Patents No. 6,781,226 ("the '226 Patent"), 7,282,951 ("the '951 Patent"), and RE42,035 ("the '035 Patent") (collectively, the "patents-in-suit"). Dkt. No. 79 at Exs. 1–3. Plaintiff submits: "The innovations in the Asserted Patents relate to developments into a new type of IC, which allows for a compact processor module with increased data speeds and processing efficiency. For example, the innovations of the Asserted Patents allow for a large number of connections between adjacent semiconductor regions, using connection techniques such as through-silicon vias ('TSVs'), to provide contacts that dramatically increase efficiency of the connections. The Asserted Patents are directed to ICs that include[] a 'programmable array.' Generally, the IC die connects components through multiple contact points." Dkt. No. 79 at 1.

The '226 Patent, titled "Reconfigurable Processor Module Comprising Hybrid Stacked Integrated Circuit Die Elements," issued on August 24, 2004, and bears an earliest priority date of December 5, 2001. The Abstract of the '226 Patent states:

> A reconfigurable processor module comprising hybrid stacked integrated circuit ("IC") die elements. In a particular embodiment disclosed herein, a processor module with reconfigurable capability may be constructed by stacking one or more thinned microprocessor, memory and/or field programmable gate array ("FPGA") die elements and interconnecting the same utilizing contacts that traverse the thickness of the die. The processor module disclosed allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost.

The '951 Patent issued on October 16, 2007, and resulted from a continuation of a continuation-in-part of the '226 Patent. The '226 Patent resulted from a continuation of United States Patent Application No. 10/012,057, filed on December 5, 2001, which issued as United States Patent No. 6,627,985 ("the '985 Patent"). The '035 Patent is a reissue of the '985 Patent,

and Plaintiff submits that the reissue "correct[ed] simple typographical errors in Claims 3 and 11" in which "a term lack[ed] an antecedent basis." Dkt. No. 79 at 7. Plaintiff also submits that "[t]he Asserted Patents all share a similar specification, and all include claims that are generally directed to different configurations of components on an IC." *Id*. at 2.

Plaintiff has asserted Claims 13, 14, 16–23, and 25–30 of the '226 Patent, Claims 1, 4, 5, 8, 10, and 13–15 of the '951 Patent, and Claims 1, 3, 5, 6–9, 11, 13–17, 19–22, 25, 26, 28, and 29 of the '035 Patent. *Id*.

Shortly before the start of the November 10, 2020 hearing, the Court provided the parties with preliminary constructions with the aim of focusing the parties' arguments and facilitating discussion. Those preliminary constructions are noted below within the discussion for each term.

II. LEGAL PRINCIPLES

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). Claim construction is clearly an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970–71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). "In some cases, however, the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period." *Teva*, 135 S. Ct. at 841 (citation omitted). "In cases where those subsidiary facts are in dispute, courts will need to make subsidiary factual findings about that extrinsic evidence. These are the 'evidentiary underpinnings' of claim construction that we discussed in *Markman*, and this subsidiary factfinding must be reviewed for clear error on appeal." *Id.* (citing 517 U.S. 370).

To determine the meaning of the claims, courts start by considering the intrinsic evidence. *See Phillips*, 415 F.3d at 1313; *see also C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1314; *C.R. Bard*, 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. *Phillips*, 415 F.3d at 1312–13; *accord Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. *Phillips*, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can aid in determining the claim's meaning because claim terms are typically used consistently throughout the patent. *Id*. Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id*. at 1315 (quoting *Markman*, 52 F.3d at 979). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Phillips*, 415 F.3d at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *accord Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. In these situations, the inventor's lexicography governs. *Id*. The

specification may also resolve the meaning of ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex*, 299 F.3d at 1325. But, "[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims." *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *accord Phillips*, 415 F.3d at 1323.

The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. *Home Diagnostics, Inc. v. Lifescan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent."). "[T]he prosecution history (or file wrapper) limits the interpretation of claims so as to exclude any interpretation that may have been disclaimed or disavowed during prosecution in order to obtain claim allowance." *Standard Oil Co. v. Am. Cyanamid Co.*, 774 F.2d 448, 452 (Fed. Cir. 1985).

Although extrinsic evidence can be useful, it is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Phillips*, 415 F.3d at 1317 (citations and internal quotation marks omitted). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a

term's definition are entirely unhelpful to a court. *Id.* Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*.

The Supreme Court of the United States has "read [35 U.S.C.] § 112, ¶ 2 to require that a patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014). "A determination of claim indefiniteness is a legal conclusion that is drawn from the court's performance of its duty as the construer of patent claims." *Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1347 (Fed. Cir. 2005) (citations and internal quotation marks omitted), *abrogated on other grounds by Nautilus*, 134 S. Ct. 2120.

III. AGREED TERMS

In their August 18, 2020 Joint P.R. 4-3 Claim Construction and Prehearing Statement, the parties submit that "[t]he parties do not agree to the construction of any identified claim term." Dkt. No. 58 at 1.

IV. DISPUTED TERMS

A. "means for reconfiguring the programmable array within one clock cycle" and "means for updating the plurality of configuration logic cells within one clock cycle"

"means for reconfiguring the programmable array within one clock cycle" ('226 Patent, Claim 13)	
Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
Governed by 35 U.S.C. § 112(6): Function: "reconfiguring the programmable array within one clock cycle" Structure: "a wide configuration data port"	Governed by 112, ¶ 6 Function: "reconfiguring the programmable array within one clock cycle" Structure: "a wide configuration data port interconnecting a stacked memory die and FPGA die using contact points distributed throughout the dies" Otherwise indefinite
"means for updating the plurality of configuration logic cells within one clock cycle" ('226 Patent, Claim 22)	
Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
Governed by 35 U.S.C. § 112(6): Function: "updating the plurality of configuration logic cells within one clock cycle" Structure: "a wide configuration data port"	Governed by 112, ¶ 6 Function: "updating the plurality of configuration logic cells within one clock cycle" Structure: "a wide configuration data port interconnecting a stacked memory die and FPGA die using contact points distributed throughout the dies" Otherwise indefinite

Dkt. No. 79 at 9–10; Dkt. No. 91 at 3; Dkt. No. 97 at 1; Dkt. No. 104, Ex. A at 1–2; *see* Dkt. No. 58 at 7 & 10.

Shortly before the start of the November 10, 2020 hearing, the Court provided the parties with the following preliminary constructions:

Term	Preliminary Construction
"means for reconfiguring the programmable array within one clock cycle" ('226 Patent, Claim 13)	Governed by 35 U.S.C. § 112, ¶ 6 Function: "reconfiguring the programmable array within one clock cycle" Structure: "wide configuration data port 82, and contact points formed throughout the area of each die element; and equivalents thereof"
"means for updating the plurality of configuration logic cells within one clock cycle" ('226 Patent, Claim 22)	Governed by 35 U.S.C. § 112, ¶ 6 Function: "updating the plurality of configuration logic cells within one clock cycle" Structure: "wide configuration data port 82, and contact points formed throughout the area of each die element; and equivalents thereof"

(1) The Parties' Positions

Plaintiff argues that "the parties' disagreement regarding this term lies in Samsung's attempt to add additional structure beyond a wide configuration data port, including structures that are not explicitly and 'clearly linked' to the recited functions." Dkt. No. 79 at 10 (quoting *B. Braun Med. Inc., v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997)); *see* also *id.* at 12–13. Plaintiff also argues that Defendants' proposal "impermissibly makes dependent Claims 14 and 23 have a broader construction than Claims 13 and 22, the independent claims they depend from." *Id.* at 13.

Further, Plaintiff argues that Defendants' indefiniteness argument should be rejected based on the opinions of Plaintiff's expert and because "Samsung's indefiniteness allegation is inherently contradictory, as Samsung has offered a construction for these elements." *Id*. at 13–14. Finally, Plaintiff submits that in recent *Inter Partes* Review ("IPR") proceedings, "Samsung construed this claim and did not argue it was indefinite." *Id*. at 14. Plaintiff cites the opinions of Samsung's expert in the IPR proceedings. *See id*., Ex. 7, May 29, 2020 Shanfield Decl. at ¶¶ 50–54.

Defendants respond that "the specifications demonstrate that the data port requires an interconnection structure between a memory die and an FPGA die to effectuate the reconfiguring/updating function." Dkt. No. 91 at 3. Defendants submit that "the only structure mentioned in the specification of the '226 patent that reconfigures within one clock cycle involves an FPGA, particularly the FPGA of Figs. 4 and 5," and "a critical structure disclosed for reconfiguring within one clock cycle is the specific connection between the memory and FPGA die, as disclosed in Figs. 4 and 5." *Id.* at 4 & 5. Defendants urge that "[t]he '226 patent unambiguously explains that the structure required to reconfigure (or update) the FPGA in parallel must include a stacked memory die and FPGA die interconnected by contact points distributed throughout the dies." *Id*. at 6. Defendants argue that Plaintiff's proposed corresponding structure, without more, fails to "distinguish a 'wide' configuration data port from a conventional one, making it impossible to ascertain what, under Arbor's view, constitutes 'wide.'" *Id*. at 7.

Plaintiff replies that "'wide' refers to the fact that it is applied to a broader set of cells, allowing an update to be performed in one clock cycle, which was not possible with a data port that is not 'wide.'" Dkt. No. 97 at 2.

At the November 10, 2020 hearing, the parties presented no oral argument and submitted this disputed term on the briefing.

(2) Analysis

Title 35 U.S.C. § 112, ¶ 6[1] provides: "An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." The Federal Circuit has provided that "[i]n exchange for using this form of claiming, the patent specification must disclose with sufficient particularity the corresponding structure for performing the claimed function and *clearly link* that structure to the function." *Triton Tech of Tex., LLC v. Nintendo of Am., Inc.*, 753 F.3d 1375, 1378 (Fed. Cir. 2014) (emphasis added).

Claims 13 and 14 of the '226 Patent recite (emphasis added):

> 13. A processor module comprising:
> at least a first integrated circuit die element including a programmable array;
> at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;
> at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and
> *means for reconfiguring the programmable array within one clock cycle*.
>
> 14. The processor module of claim 13 wherein the reconfiguring means comprises a wide configuration data port.

Claims 22 and 23 of the '226 Patent recite (emphasis added):

> 22. A processor module comprising:
> at least a first integrated circuit die element including a programmable array and a plurality of configuration logic cells;
> at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;
> at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and

[1] This provision is also known as 35 U.S.C. § 112(f).

> *means for updating the plurality of configuration logic cells within one clock cycle*.
>
> 23. The processor module of claim 22 wherein the updating means comprises a wide configuration data port.

The parties agree that the claimed functions are "reconfiguring the programmable array within one clock cycle" and "updating the plurality of configuration logic cells within one clock cycle." The parties also agree that the corresponding structure includes a "wide configuration data port," but the parties otherwise dispute the proper corresponding structure. Plaintiff argues that Defendants' proposal of referring to "interconnecting a stacked memory die and FPGA die using contact points distributed throughout the dies" is not directly linked to the recited function. Dkt. No. 79 at 11.

The specification discloses:

> With reference additionally now to FIG. 5, a corresponding functional block diagram of the configuration cells 80 of the reconfigurable processor module 60 of the preceding figure is shown wherein the FPGA 70 may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel. As opposed to the conventional implementation of FIG. 3, a *wide configuration data port 82* is included to *update the various logic cells 84* through an associated configuration memory 86 and buffer cell 88. The buffer cells 88 are preferably a portion of the memory die 66 (FIG. 4). In this manner, they can be loaded while the FPGA 68 comprising the logic cells 84 are in operation. This then enables the FPGA 68 to be totally reconfigured *in one clock cycle* with all of it[s] configuration logic cells 84 *updated in parallel*. Other methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory ("RAM") than can be offered within the FPGA die 68 itself.

'226 Patent at 4:45–59 (emphasis added); *see also id.* at 3:33–37 ("FIG. 5 is a corresponding functional block diagram of the configuration cells of the reconfigurable processor module of FIG. 4 wherein the FPGA may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel.").

The specification thus links the claimed functions to the particular "wide configuration data port 82" that is disclosed. *See id*. at 4:45–59; *see also id*. at Fig. 5.

Defendants cite disclosure regarding contact points formed throughout the areas of dies[2] such as a microprocessor die, a memory die, and an FPGA die:

> With reference additionally now to FIG. 4, a simplified, exploded isometric view of a reconfigurable processor module 60 in accordance with a representative embodiment of the present invention is shown comprising a hybrid device incorporating a number of stacked integrated circuit die elements. In this particular implementation, the module 60 comprises a die package 62 to which is coupled a microprocessor die 64, memory die 66 and FPGA die 68, all of which have a number of corresponding *contact points*, or holes[] 70[,] formed throughout the area of the package 62 and various die 64, 66 and 68.

'226 Patent at 4:10–20 (emphasis added).

Defendants highlight this reference to an FPGA, but the claimed functions refer to "*reconfiguring* the programmable array within one clock cycle" and "*updating* the plurality of configuration logic cells within one clock cycle." These functions do not refer to any operation carried out *by* the programmable array itself. The Court therefore rejects Defendants' proposal of requiring the corresponding structure to include an FPGA. Also, the parties present "programmable array" as a separate disputed term, which is addressed separately below.

Defendants cite IPR proceedings in which Plaintiff distinguished prior art references, such as by Plaintiff arguing that "shifting a memory plane into an FPGA function is not synonymous with, and does not teach, reconfiguring an FPGA in one clock cycle, as required by Claim 13." Dkt. No. 91, Ex. B, IPR 2020-01022 ('226 Patent), Sept. 4, 2020 Patent Owner's Preliminary Response at 21. Plaintiff's discussion of an FPGA, however, was responsive to the petitioner's

[2] In the semiconductor industry, the plural of "die" is sometimes referred to as "dice" but perhaps is more commonly referred to as "dies," which is the plural form that the parties used at the November 10, 2020 hearing.

argument that identified an FPGA as an *example* of a programmable array. *See id*. at 20 ("Petitioner alleges that '[r]econfiguring a programmable array (such as an FPGA) in one clock cycle was well-known in the art and disclosed in [the] Cooke [reference].'"); *see also id*. ("Cooke does *not* describe '"nearly instantaneous configuration" of an FPGA' as Petitioner suggests.").

This prosecution history therefore does not contain any definitive statement, definition, disclaimer, or disavowal that would warrant requiring an FPGA as part of the corresponding structure. The opinions of Defendants' expert in this regard do not compel otherwise. *See* Dkt. No. 91, Ex. A, Oct. 13, 2020 Liu Decl. at ¶¶ 71–76.

Likewise, Defendants fail to adequately support their proposal that the corresponding structure must refer to a "stacked" memory die, and the parties present "stacked with and electrically coupled to" as a distinct disputed term, which is addressed below.

As to Defendants' proposal regarding "contact points," Defendants argue that a "contact points" interface structure is necessary to perform the claimed function because otherwise the data port would be unable to perform the reconfiguring/updating in one clock cycle. *See* Dkt. No. 91 at 3–4 & 5–7. The above-reproduced disclosure regarding Figure 4 refers to "contact points, or holes[] 70[,] formed throughout the area of the package 62 and various die 64, 66 and 68." '226 Patent at 4:10–20; *see also id*. at 5:18–29. This disclosure regarding Figure 4 refers to the same embodiment as the above-reproduced disclosure regarding Figure 5, which refers to the "wide configuration data port 82." *See id*. at 4:55–50 ("of the preceding figure"); *see also id*. at 3:33–37 ("*FIG. 5* is a corresponding functional block diagram of the configuration cells of the reconfigurable processor module *of FIG. 4* wherein the FPGA may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel.") (emphasis added).

Reading these disclosures as a whole, and considering that the claimed functions do not merely recite reconfiguring or updating in general but rather recite doing so within one clock cycle, the corresponding structure includes the above-discussed "contact points" (also referred to in the specification as "contacts"). *See* '226 Patent at 4:10–20 & 5:16–24. The contrary opinion of Plaintiff's expert does not compel otherwise. *See* Dkt. No. 80-1, Sept. 29, 2020 Darveaux Decl. at ¶ 16.

Plaintiff's statements in IPR proceedings reinforce this understanding. In a discussion of the "Koyanagi" reference and the "Cooke" reference, Plaintiff argued that "vertical connections between stacked chips have many uses and the mere existence of such interconnections does not mean that the *interconnections* are structured as a *wide configuration data port*." Dkt. No. 91, Ex. B, IPR 2020-01022, Sept. 4, 2020 Patent Owner's Preliminary Response at 19 (emphasis added). Plaintiff's understanding of wide configuration data ports thus appears to include particular types of interconnections, such as the above-discussed "contact points." Plaintiff also argued as follows:

> Indeed, as discussed with respect to Fig. 5 of the '226 Patent, while *the wide configuration data port takes advantage of die-area connections*, its structure, which facilitates "updating all of the configuration cells in parallel" *thereby* enabling "the FPGA 68 to be totally *reconfigured* in one clock cycle" represents a *novel arrangement* theretofore not known in the art and which Petitioner has not established to be an obvious modification of the combination of Koyanagi and Cooke.

Id. at 24 (emphasis modified). Plaintiff argues that "Arbor's statements were not made in the context of defining these means-plus-function elements, and did not state that this was required," Dkt. No. 97 at 3, but Plaintiff fails to adequately explain why these above-reproduced statements regarding the disclosure at issue should not be considered to at least some degree.[3]

[3] Defendants further offer the recent construction of these terms by the PTAB (Dkt. No. 154), which the Court has taken into account.

Finally, Plaintiff cites the doctrine of claim differentiation. *See, e.g.*, *RF Del., Inc. v. Pac. Keystone Techs., Inc.*, 326 F.3d 1255, 1264 (Fed. Cir. 2003) ("An independent claim usually covers a scope broader than the preferred embodiment, especially if the dependent claims recite the precise scope of the preferred embodiment."); *Phillips*, 415 F.3d at 1315 ("the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim"). Plaintiff's reliance on claim differentiation as to dependent Claims 14 and 23 (reproduced above) is unavailing because the terms here at issue are means-plus-function terms and the "contact points" structure "comes from the specification via section 112(6)." *Laitram Corp. v. Rexnord, Inc.*, 939 F.2d 1533, 1538 (Fed. Cir. 1991) ("the judicially developed guide to claim interpretation known as 'claim differentiation' cannot override the statute").

In its reply brief, Plaintiff challenges Defendants' reliance on *Laitram*, *id*., and Plaintiff cites authority that "it does not necessarily follow that means-plus function limitations must be interpreted without regard to other claims." *Wenger Mfg. v. Coating Mach. Sys.*, 239 F.3d 1225, 1233 (Fed. Cir. 2001). *Wenger* itself, however, also stated that "the judicially created doctrine of claim differentiation cannot override the statutory requirements of § 112, ¶ 6," and "claim differentiation is not a hard and fast rule of construction[] and cannot be relied upon to broaden claims beyond their correct scope." *Id*. (citations and internal quotation marks omitted). *Wenger* applied the doctrine of claim differentiation to find that a dependent claim recited "a separate and distinct *function*." *Id*. at 1234 (emphasis added); *see also id*. ("[T]he doctrine of claim differentiation supports the conclusion that the 'air circulation means' limitation in claim 1 should be limited to structure for performing the recited function of circulating air, and should not be

interpreted as requiring structure capable of performing the additional function of recirculation, which is expressly recited in dependent claim 3 and not found in claim 1.").

Wenger therefore does not compel reliance on the doctrine of claim differentiation when determining the proper corresponding structure in the present case. Plaintiff's attempt to do so in the present case should be rejected.

Plaintiff's reliance on the doctrine of claim differentiation as to dependent Claims 19 and 28 (which recite that the "die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements") in its reply brief, Dkt. No. 97 at 2, is unavailing for the same reasons set forth above regarding dependent Claims 14 and 23. *See Laitram*, 939 F.2d at 1538. Indeed, *Wenger* expressly noted that *Laitram*, *id*., "held that the stringencies of a means-plus-function limitation are not to be avoided by the mere addition of a dependent claim that recites the corresponding structure disclosed in the specification." 239 F.3d at 1234.

The Court therefore hereby construes these disputed terms as set forth in the following chart:

Term	Construction
"means for reconfiguring the programmable array within one clock cycle"	**Governed by 35 U.S.C. § 112, ¶ 6** Function: **"reconfiguring the programmable array within one clock cycle"** Structure: **"wide configuration data port 82, and contact points formed throughout the area of each die element; and equivalents thereof"**

"means for updating the plurality of configuration logic cells within one clock cycle"	**Governed by 35 U.S.C. § 112, ¶ 6** Function: **"updating the plurality of configuration logic cells within one clock cycle"** Structure: **"wide configuration data port 82, and contact points formed throughout the area of each die element; and equivalents thereof"**

B. "processor module"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
Preamble is not limiting. No construction necessary – Plain and ordinary meaning which is a module that performs processing[4]	The Preamble is limiting. "hybrid bare integrated circuit die elements, including a processor, stacked into a single block and electrically interconnected"

Dkt. No. 58 at 13; Dkt. No. 91 at 8; Dkt. No. 97 at 3; *see* Dkt. No. 79 at 14–15; *see also* Dkt. No. 104, Ex. A at 2–3. The parties submit that this term appears in Claims 13, 14, 16–23, and 25–30 of the '226 Patent, Claims 1, 4, 5, 10, and 13–15 of the '951 Patent, and Claims 1, 3, 5–9, 17, 19–22, 25, 26, 28, and 29 of the '035 Patent. Dkt. No. 58 at 13; Dkt. No. 104, Ex. A at 2–3.

Shortly before the start of the November 10, 2020 hearing, the Court provided the parties with the following preliminary construction: "In the Preambles: Not limiting"; and "As to '951 Patent Claim 5 and '035 Patent Claim 9: "module that includes a processor or that has processing capability."

[4] Plaintiff previously proposed: "Plain and ordinary meaning." Dkt. No. 58 at 13; Dkt. No. 79 at 14–15.

(1) The Parties' Positions

Plaintiff argues that this term, where it appears only in the preambles, is not limiting because "the term 'processor module' simply describes the general type of component (*e.g.*, a module that performs processing), and does not add anything to the claims that would aid in their interpretation or understanding." Dkt. No. 79 at 15.[5] As to Defendants' proposed construction, Plaintiff argues that "'[h]ybrid bare' is not used at all in the specification," and for "'stacked into a single block,' the claims already set forth when and what components in the claims are stacked, and, therefore, Samsung's inclusion of this language would deviate from a plain reading of the claim language." *Id.* at 16.

Defendants respond that these preambles are limiting because "[t]he patents describe the purported invention as a 'processor module,' and emphasize the required structural configuration from beginning to end." Dkt. No. 91 at 8. Defendants cite "repeated usage" of "processor module" in the Titles, Abstracts, and specifications of the patents-in-suit. *Id*. at 8–9. As to the proper construction, Defendants argue that: (1) "[t]he term 'module' precludes a collection of discrete and disconnected components"; (2) "the claims do not cover just any type of 'module;' rather, they cover a 'processor' module"; and (3) "[e]xcluding 'processor' from 'processor module' makes no sense." *Id.* at 10.

Plaintiff replies that "[i]n nearly all of the claims, 'processor module' is found only in the preamble of the claims and not referred to in the body, thus demonstrating that the processing module does not breathe life and meaning into the claims, and should not be considered a

[5] The term "processor module" appears in the bodies of Claim 5 of the '951 Patent and Claim 9 of the '035 Patent, as Plaintiff acknowledges. Dkt. No. 79 at 16 n.4. As to those claims, Plaintiff does not dispute that the term "processor module" is limiting. Instead, Plaintiff argues that "the two claims that include this term in their body already define a 'processor module.'" *Id*. at 16.

limitation." Dkt. No. 97 at 3. Plaintiff also argues that "the use of 'present invention' cannot be used to make the preamble a limitation, as the specification discloses multiple different 'present inventions' in the specification." *Id.* at 4. Further, Plaintiff argues that "in each case where 'processor module' is used in the body of the claims, it is always explicitly defined in the claims themselves, and setting forth the plain understanding of the terms." *Id.*

At the November 10, 2020 hearing, the parties reiterated the arguments set forth in their briefing.

(2) Analysis

> In general, a preamble limits the invention if it recites essential structure or steps, or if it is "necessary to give life, meaning, and vitality" to the claim. *Pitney Bowes*[, *Inc. v. Hewlett-Packard Co.*], 182 F.3d [1298,] 1305 [(Fed. Cir. 1999)]. Conversely, a preamble is not limiting "where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention." *Rowe v. Dror*, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997).

Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 808 (Fed. Cir. 2002); *see, e.g.*, *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003) ("When limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention."); *C.W. Zumbiel Co. v. Kappos*, 702 F.3d 1371, 1385 (Fed. Cir. 2012) (finding preambles limiting because "'containers' as recited in the claim body depend on 'a plurality of containers' in the preamble as an antecedent basis").

Also, "the purpose or intended use of the invention . . . is of no significance to claim construction . . . ." *See Pitney Bowes*, 182 F.3d at 1305. This principle has sometimes been characterized as "the presumption against reading a statement of purpose in the preamble as a claim limitation." *Marrin v. Griffin*, 599 F.3d 1290, 1294–95 (Fed. Cir. 2010); *see Allen Eng'g Corp. v. Bartell Indus.*, 299 F.3d 1336, 1346 (Fed. Cir. 2002) ("Generally, the preamble does not

limit the claims."); *see also Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 769–71 (Fed. Cir. 2018) (in preamble reciting "[a] computer network for providing an information delivery service for a plurality of participants," finding "information delivery service" to be non-limiting because it "merely describe[s] intended uses for what is otherwise a structurally complete invention").

As Plaintiff submits, the term "processor module" appears in *either* the preamble *or* the body of each claim, so there is *no* claim in which the term "processor module" appears in *both* the preamble and the body of the claim. As to the claims that recite "processor module" in the body of the claim, namely Claim 5 of the '951 Patent and Claim 9 of the '035 Patent, Plaintiff does not contest that the term "processor module" is limiting in those claims. Dkt. No. 79 at 16. As to the other claims, in which the term "processor module" appears only in the preamble, Claim 13 of the '226 Patent is representative and recites (emphasis added):

> 13. A *processor module* comprising:
> at least a first integrated circuit die element including a programmable array;
> at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;
> at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and
> means for reconfiguring the programmable array within one clock cycle.

The preamble of Claim 25 of the '035 Patent differs slightly from the other claims at issue by reciting a "reconfigurable" processor module (emphasis added):

> 25. A *reconfigurable processor module* comprising:
> at least a first integrated circuit die element including a programmable array;
> at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element; and
> at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively

whereby said processor and said programmable array are operational to share data therebetween.

Defendants also cite *On Demand Machine Corp.* for the proposition that a preamble is limiting if it states a "fundamental characteristic of the claimed invention," "serves to focus the reader on the invention that is being claimed," or "states the framework of the invention." *On Demand Mach. Corp. v. Ingram Indus., Inc.*, 442 F.3d 1331, 1343 (Fed. Cir. 2006). Defendants also cite *Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1358 (Fed. Cir. 2012), and Defendants point to "repeated usage" of the term "processor module" in the Titles, Abstracts, and specifications of the patents-in-suit. Dkt. No. 91 at 8–9. Also, *Deere* pointed to a feature being "underscored as important by the specification." 703 F.3d at 1358 (quoting *Catalina*, 289 F.3d at 808). Additionally, in some cases, "[w]hen a patent . . . describes the features of the 'present invention' as a whole, this description limits the scope of the invention." *Forest Labs., LLC v. Sigmapharm Labs., LLC*, 918 F.3d 928, 933 (Fed. Cir. 2019) (quoting *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007)).

First, the Titles and Abstracts of the patents-in-suit refer to a "processor module." Second, the Background of the Invention states that "the present invention relates to an extremely compact reconfigurable *processor module* comprising hybrid stacked integrated circuit ('IC') die elements." '226 Patent at 1:15–18 (emphasis added). Third, the Summary of the Invention refers to a "new processor module." *Id.* at 2:19–21; *see id.* at 2:40–43. Fourth, the specification refers to a "processor," "processor module," or "microprocessor" in several instances. *See id.* at 4:10–20, 4:20–24, 4:34–39, 4:45–50 & 5:5–10.

Yet, these characterizations of the claimed inventions and these disclosures regarding what the claimed inventions "relate[] to" (*id.* at 1:15–18) do not justify departing from the usual principle that when the preamble does not provide antecedent basis and is merely "descriptive" of

the limitations set forth in the body of the claim, the preamble is not limiting. *IMS Tech., Inc. v. Haas Automation, Inc.*, 206 F.3d 1422, 1434 (Fed. Cir. 2000) ("The phrase 'control apparatus' in the preamble merely gives a descriptive name to the set of limitations in the body of the claim that completely set forth the invention."); *see Catalina*, 289 F.3d at 808 ("patentee defines a structurally complete invention in the claim body") (citation omitted).

The *Poly-America* and *General Electric* cases cited by Defendants are likewise unpersuasive. *See Poly-Am., L.P. v. GSE Lining Tech., Inc.*, 383 F.3d 1303, 1310 (Fed. Cir. 2004); *see also Gen. Elec. Co. v. Nintendo Co.*, 179 F.3d 1350, 1361–62 (Fed. Cir. 1999). In sum, this is *not* a case in which the patentee "use[d] *both* the preamble and the body to define the subject matter of the claimed invention." *Bell Commc'ns Research, Inc. v. Vitalink Commc'ns Corp.*, 55 F.3d 615, 620 (Fed. Cir. 1995).

The Court therefore finds that the term "processor module," in the preambles of the claims here at issue, is not limiting.

As to Claim 5 of the '951 Patent and Claim 9 of the '035 Patent, in which the term "processor module" appears in the body of each claim, Claim 5 of the '951 Patent recites (emphasis added):

> 5. A reconfigurable computer system comprising:
>
> a processor;
>
> a memory; and
>
> at least one *processor module* including at least a first integrated circuit functional element having a programmable array that is programmable as a processing element and at least a second integrated circuit functional element that includes a memory array stacked with and electrically coupled to said programmable array of said first integrated circuit functional element wherein said memory array is functional to accelerate external memory references to the processing element.

Claim 9 of the '035 Patent recites (emphasis added):

> 9. A reconfigurable computer system comprising:

> a processor;
> a memory;
> at least one *processor module* including at least a first integrated circuit die element having a programmable a [*sic*] array and at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element; and
> wherein said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements, and wherein said contact points traverse said die elements through a thickness thereof.

These claims thus expressly recite various limitations regarding the "processor module." Defendants propose limiting the "processor module" to being "hybrid bare integrated circuit die elements, including a processor, stacked into a single block and electrically interconnected."

As to Defendants' proposals of "integrated circuit die elements" and "stacked into a single block and electrically interconnected," the above-reproduced claims already contain other claim language directed to such features, so Defendants' proposal would tend to be confusing or perhaps even contradictory with other claim language.

Defendants' proposal of "hybrid bare" is unclear. Disclosures regarding "hybrid" refer to combinations of integrated circuit die elements, which is already addressed by surrounding claim language. The disclosure in the Summary of the Invention that "[p]articularly disclosed herein is a processor module with reconfigurable capability constructed by stacking and interconnecting *bare* die elements" ('226 Patent at 2:41–43 (emphasis added)) is insufficient to warrant introducing the word "bare," in particular because surrounding claim language already expressly addresses die elements. Defendants cite statements by Plaintiff in IPR proceedings that "[t]he innovations in the '226 Patent relate to a new type of IC called a 'stacked die hybrid ('SDH') processor" and "[t]he SDH processor uses a wide number of direct connections between adjacent semiconductor dies," but these do not amount to any definitive statement, definition, disclaimer, or disavowal that would justify the construction of "processor module" proposed here by Defendants. Dkt. No. 91, Ex. B,

IPR 2020-01022 ('226 Patent), Sept. 4, 2020 Patent Owner's Preliminary Response at 1–2; *see id.*, Ex. E at 1–2; *see also id.*, Ex. F, at 1–2.

Finally, as to Defendants' proposal of "including a processor," the term itself already recites that the module is a "processor" module, and the technical definitions of "module" cited by Defendants do not compel requiring such a module to include a "processor." *See* Dkt. No. 91, Ex. C, *Microsoft Computer Dictionary* 346 (5th ed. 2002) ("In hardware, a self-contained component that can provide a complete function to a system and can be interchanged with other modules that provide similar functions."); *see also id.*, Ex. D, *Dictionary of Computer and Internet Words* 177 (2001) ("A self-contained hardware component that is installed as a unit."). Instead, the word "processor" can be given proper effect by requiring a module that includes a processor or that has processing capability.

For the reasons set forth above, the Court hereby finds that **"processor module"** as used in the **preambles** is **not limiting**, and

as to Claim 5 of the '951 Patent and Claim 9 of the '035 Patent, in which the term "processor module" appears in the body of each claim, the Court hereby construes:

- **"processor module"** to mean **"module that includes a processor or that has processing capability."**

C. "programmable array"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
No construction necessary – Plain and ordinary meaning which is an array of components that can be programmed with instructions[6]	"reconfigurable processor that alters its hardware complement to create the number of functional units it needs for each application in hardware"

[6] Plaintiff previously proposed: "Plain and ordinary meaning." Dkt. No. 58 at 16; *see* Dkt. No. 79 at 17.

Dkt. No. 58 at 16; Dkt. No. 91 at 11; Dkt. No. 97 at 5; *see* Dkt. No. 79 at 17; *see also* Dkt. No. 104, Ex. A at 3. The parties submit that this term appears in Claims 13, 18, 22, and 27 of the '226 Patent, Claims 1, 5, 10, and 14 of the '951 Patent, and Claims 1, 7, 9, 15, 17, 21, and 25 of the '035 Patent. Dkt. No. 58 at 16–17; Dkt. No. 104, Ex. A at 3.

On November 10, 2020, the Court provided no preliminary construction for this disputed term.

(1) The Parties' Positions

Plaintiff argues that "[b]ecause the '226 Patent does not use special terminology, no construction is required." Dkt. No. 79 at 17. Plaintiff also argues that "the patentee did not set forth a specific definition of 'programmable array' in the specification that would limit the meaning of this term," and "the specification and prosecution history of the '226 Patent demonstrate that the patentee did not limit 'programmable array' or make any representations regarding this term in order to avoid the prior art." *Id*. at 18. Plaintiff urges that "Samsung's proposed construction improperly seeks to limit the 'programmable array' to a specific embodiment with a processor," and Plaintiff also argues claim differentiation as between independent Claim 13 and dependent Claim 18 and between independent Claim 22 and dependent Claim 27. *Id*. at 19. Plaintiff argues that "given the intrinsic evidence, a 'programmable array' cannot be construed to be the same thing as a processor or reconfigurable processor." *Id*. at 20. Finally, Plaintiff submits that "the examiner recognized that a programmable memory such an EEPROM is a 'programmable array.'" *Id*. at 21.[7]

[7] Plaintiff also cites the opinion of one of Defendants' experts in an IPR proceeding, which Plaintiff characterizes as an opinion that this term should be given its plain and ordinary meaning (Dkt. No. 79 at 17), but the cited opinion merely explains the position of Defendants' expert that no construction is necessary as to the non-means terms because: "[I]t is my opinion that for purposes of this proceeding, except for the 'means' terms, no other terms need be construed to resolve the prior art issues presented in this Petition. This is because, as detailed in Section X, each of the prior

Defendants respond that Plaintiff's proposal "offers a construction that seeks to capture[] the very types of devices the patents disparage, such as a microprocessor or memory." Dkt. No. 91 at 11. Defendants note that the claims recite a memory and a microprocessor as distinct from a programmable array, and "[n]owhere does the specification use the term 'programmable' or 'program,' let alone 'programmable array,' with components such as memory or microprocessors." *Id*. at 12–13. Defendants submit that "FPGAs are the sole disclosed example of 'programmable array' in the claims, and FPGAs are the sole disclosed example of 'reconfigurable processors' in the specification." *Id*. at 13. Defendants emphasize that the specification refers to the present invention as relating to a reconfigurable processor, which is a processor that "alters its hardware complement to create the number of functional units it needs for each application in hardware (in stark contrast to memory or microprocessors)." *Id*. at 14. Defendants argue that "[i]f not for Samsung's proposed construction, the claims would not even arguably solve the problems the patents identify." *Id*. at 15 (footnote omitted).

Plaintiff replies that these are "readily understood words," and "[f]or example, Claim 18 of the '951 Patent provides that the reconfigurable processor includes a programmable array, not that they are the same thing." Dkt. No. 97 at 5. Plaintiff also argues that "[e]ven the case law cited by Samsung makes it clear that the use of 'present invention' can only limit the claims when it is explicit that there is only one invention described in the specification." *Id.* at 6 (citing *Regents of Univ. of Minn. v. AGA Med. Corp.*, 717 F.3d 929, 936 (Fed. Cir. 2013)).

At the November 10, 2020 hearing, Defendants submitted that of the 97 total claims in the patents-in-suit, not a single claim recites a memory (or a microprocessor) as being the claimed

art grounds teaches, in relevant part, the exact same combination of features found in the only embodiment of the '226 Patent." Dkt. No. 79, Ex. 7, May 29, 2020 Shanfield Decl. at ¶ 53.

"programmable array."[8] Plaintiff argued that this disputed term can refer to memory, and Plaintiff emphasized that Claim 23 of the '951 Patent recites a "programmable array module" including an FPGA and a memory array.

(2) Analysis

Claim 13 of the '226 Patent, for example, recites (emphasis added):

> 13. A processor module comprising:
> at least a first integrated circuit die element including a *programmable array*;
> at least a second integrated circuit die element including a *processor* stacked with and electrically coupled to said *programmable array* of said first integrated circuit die element;
> at least a third integrated circuit die element including a memory stacked with and electrically coupled to said *programmable array* and said processor of said first and second integrated circuit die elements respectively; and
> means for reconfiguring the *programmable array* within one clock cycle.

The separate recital of a "processor" as part of the "second integrated circuit die element" weighs against Defendants' proposal that the "programmable array" in the "first integrated circuit die element" necessarily includes a processor. *See Phillips*, 415 F.3d at 1314 ("the claims themselves provide substantial guidance as to the meaning of particular claim terms"). Claim 22 of the '226 Patent is similar in this regard.

Plaintiff also cites dependent Claims 18 and 27 of the '226 Patent, which depend from independent Claims 13 and 22, respectively. Claims 18 and 27 recite:[9]

---

[8] At the November 10, 2020 hearing, Defendants also presented portions of a rough transcript of the November 8, 2020 deposition of one of the named inventors. *See* Dkt. No. 122-1 at 54–55 (Defendants' presentation slides); *see also* Dkt. No. 116-1 (transcript).) Such testimony is of little, if any, relevance in these claim construction proceedings. *See Howmedica Osteonics Corp. v. Wright Med. Tech., Inc.*, 540 F.3d 1337, 1346–47 (Fed. Cir. 2008) (noting that inventor testimony is "limited by the fact that an inventor understands the invention but may not understand the claims, which are typically drafted by the attorney prosecuting the patent application").

[9] Plaintiff also cites Claims 15 and 24 of the '226 Patent, which are dependent claims reciting that the programmable gate array "comprises a field programmable gate array." Dkt. No. 79 at 20.

> 18. The processor module of claim 13 wherein said programmable array is configurable as a processing element.
>
> * * *
>
> 27. The processor module of claim 22 wherein said programmable array is configurable as a processing element.

Plaintiff asserts the doctrine of claim differentiation, arguing that these dependent claims "narrow their respective independent claims to require that the programmable array include a processing element." Dkt. No. 79 at 19. Plaintiff concludes that a "programmable array" need not include a processor. These dependent claims, however, do not recite *including* a processing element but rather recite that the programmable array "is *configurable* as" a processing element. Nonetheless, these recitals in dependent claims that the programmable array is *configurable as* a processing element weigh at least somewhat against Defendants' suggestion that the programmable array is a processor.

The patents-in-suit do not use the term "programmable array" outside of the claims. The specification uses the word "programmable" only as part of the phrase "field programmable gate array" ("FPGA"). *See* '226 Patent at Abstract, 1:32–33 & 3:23.

At first blush, the recitals that a *field programmable gate array die element* includes a programmable array (Claim 1 of the '226 Patent) and that a "programmable array of said first integrated circuit die element *comprises* a *field programmable gate array*" (Claim 15 of the '226 Patent) could be interpreted as meaning that the patentee used "programmable array" as a synonym for referring to a field programmable gate array (FPGA). *See Phillips*, 415 F.3d at ("Other claims of the patent in question, both asserted and unasserted, can also be valuable sources of

---

Plaintiff submits that a "field programmable gate array" ("FPGA") "is a reconfigurable component that can act as a processor." *Id.* at 20 n.5.

enlightenment as to the meaning of a claim term. Because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims.") (citations omitted). Further, the acronym "FPGA" appears through the specification, both with reference to conventional implementations and with reference to the disclosed embodiments. *Compare* '226 Patent at 3:63–4:9 (configuring an FPGA "in a conventional implementation") *with id.* at 4:45–65 ("[a]s opposed to the conventional implementation," configuring an FPGA in one clock cycle).

Plaintiff does not show that the term "programmable array" has any well-established meaning in the relevant art. *See Irdeto Access, Inc. v. EchoStar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004) (holding that "absent . . . an accepted meaning [in the art], we construe a claim term only as broadly as provided for by the patent itself"). Further, in some cases, "[c]onsistent use of a term in a particular way in the specification can inform the proper construction of that term," and claim differentiation is "a guide, not a rigid rule." *Wi-LAN USA, Inc. v. Apple Inc.*, 830 F.3d 1374, 1382, 1391 (Fed. Cir. 2016) (citation and internal quotation marks omitted).

But Defendants do not propose that the term "programmable array" must refer to an FPGA (Dkt. No. 91 at 13), and dependent Claim 15 weighs at least somewhat against limiting "programmable array" to being an FPGA:

> 15. The processor module of claim 13 wherein said *programmable array* of said first integrated circuit die element comprises a *field programmable gate array*.

This "use of both terms in close proximity in the same claim gives rise to an inference that a different meaning should be assigned to each." *Bancorp Servs., LLC v. Hartford Life Ins. Co.*, 359 F.3d 1367, 1373 (Fed. Cir. 2004). Further, under the doctrine of claim differentiation, dependent Claim 15 implies that the term "programmable array" in independent Claim 13 is not

limited to a field programmable gate array (FPGA). *See Phillips*, 415 F.3d at 1315 ("the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim").

Additional dependent claims provide further context, not only above-discussed dependent Claim 15 but also Claims 16 and 17 of the '226 Patent. These claims recite (emphasis added):

> 15. The processor module of claim 13 wherein said *programmable array* of said first integrated circuit die element comprises a *field programmable gate array*.
>
> 16. The processor module of claim 13 wherein said *processor* of said second integrated circuit die element comprises a *microprocessor*.
>
> 17. The processor module of claim 13 wherein said *memory* of said third integrated circuit die element comprises a *memory array*.

These claims reinforce that a "processor," a "microprocessor," a "memory," and a "memory array" are distinct from a "programmable array."

As to Plaintiff's repeated urging in its briefing and at the November 10, 2020 hearing that the term "programmable array" can refer to memory, Plaintiff cites Claim 23 of the '951 Patent, which recites a "programmable array module" including an FPGA and a memory array. This recital of a "programmable array *module*" including certain limitations, however, does not amount to any recital of a "programmable array" *being* a "memory array."

Plaintiff also argues that the specification "describes configurable memory, which is a programmable array," and Plaintiff argues that "[t]his is shown [in] Figure 5 of the '226 Patent, which shows a programmable array of cells." Dkt. No. 79 at 18–19; *see also* Dkt. No. 97 at 6. The relevant disclosure, however, refers to "configuration memory 86" shown in Figure 5 as part of an FPGA. *See* '226 Patent at 4:45–65. This disclosure also explains that connections to a cache memory die can be used to "replace the configuration bit storage on the FPGA die 68." *Id*. A fair reading of these disclosures is that "configuration memory" can be *part of* an FPGA. Plaintiff fails

to show how this purportedly demonstrates that the term "programmable array" can be met by a configurable memory or "configuration memory." The opinion of Plaintiff's expert in this regard is merely conclusory and is therefore unpersuasive. *See* Dkt. No. 80-1, Sept. 29, 2020 Darveaux Decl. at ¶¶ 24–25.

Plaintiff cites *Acromed*, which rejected a proposal to "impermissibly import into the claim limitation specific dimensions of a preferred embodiment that are unnecessary to perform the claimed function . . .," but this analysis pertained to a means-plus-function limitation governed by 35 U.S.C. § 112, ¶ 6, which is not at issue for the term "programmable array." *Acromed Corp. v. Sofamor Danek Grp., Inc.*, 253 F.3d 1371, 1382–83 (Fed. Cir. 2001). Plaintiff fails to demonstrate that *Acromed* is applicable. Further, to whatever extent *Acromed* might be applicable, the opinion of Plaintiff's expert that "[a] POSITA would understand this term to be its plain and ordinary meaning, which is an array that can be programmed," is unpersuasive. Dkt. No. 80-1, Sept. 29, 2020 Darveaux Decl. at ¶ 23; *see id*. at ¶ 25; *see also Phillips*, 415 F.3d at 1321 (warning against "focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent").

Plaintiff also cites international prosecution history in which an examiner cited the "Corisis" reference as disclosing "at least a first integrated circuit die element (12 in Fig. 4) including a programmable array (programmable memory EEPROM . . .) . . . ." Dkt. No. 79, Ex. 8, Sept. 23, 2003 PCT Written Opinion (p. 6 of 7 of Ex. 8). Plaintiff submits that an "EEPROM" is a type of memory and is not a processor. Dkt. No. 80-1, Sept. 29, 2020 Darveaux Decl. at ¶ 26. The parties dispute whether this prosecution history can be considered and, if so, whether this prosecution history shows that the term "programmable array" encompasses memory.

Even when considered, this evidence lacks "clarity" because neither the examiner nor the patentee discussed the meaning of "programmable array" in any more detail. *Phillips*, 415 F.3d at 1317 (noting that prosecution history "often lacks the clarity of the specification and thus is less useful for claim construction purposes"). This evidence therefore does not significantly affect the Court's analysis and certainly does not override the context provided by the specification distinguishing between memory and FPGAs (Plaintiff agrees that the term "programmable array" encompasses FPGAs). *See* '226 Patent at 4:15–24. The specification discloses that FPGAs may include memory, *see id*. at 4:45–65, but FPGAs are disclosed as distinct from the disclosed "memory" dies. *See id*. at 4:14–24 & Fig. 4.[10]

As to Defendants' proposal of a "reconfigurable processor," the Background of the Invention states that "the present invention relates to an extremely compact *reconfigurable processor module* comprising hybrid stacked integrated circuit ('IC') die elements" ('226 Patent at 1:15–18 (emphasis added)), which thus refers to multiple die elements, not just the programmable array of the recited first integrated circuit die element. The Summary of the Invention similarly states:

> In accordance with the disclosure of a representative embodiment of the present invention, *FPGAs, microprocessors and cache memory may be combined* through the use of recently available wafer processing techniques to create a particularly advantageous form of hybrid, *reconfigurable processor module* that overcomes the limitations of present discrete, integrated circuit device implementations of GPRP systems. As disclosed herein, this new processor module may be conveniently denominated as a Stacked Die Hybrid ("SDH") Processor.

Id. at 2:11–21 (emphasis added).

[10] Plaintiff's reliance on prosecution history of the '951 Patent, as well as Defendants' reliance on Canadian prosecution, likewise does not significantly affect the Court's analysis. *See* Dkt. No. 79, Ex. 11, Feb. 8, 2007 Office Action at 5; *see also* Dkt. No. 91, Ex. G, Response to Official Action, at 3.

Additional discussion in the Background of the Invention, cited by Defendants themselves, further weighs against Defendants' proposal that a "programmable array" is a reconfigurable processor:

> In addition to current commodity IC microprocessors, another type of processing element is commonly referred to as a reconfigurable, or adaptive, processor. These reconfigurable processors exhibit a number of advantages over commodity microprocessors in many applications. Rather than using the conventional "load/store" paradigm to execute an application using a set of limited functional resources as a microprocessor does, the reconfigurable processor actually creates the number of functional units it needs for each application in hardware. This results in greater parallelism and, thus, higher throughput for many applications. Conventionally, *the ability for a reconfigurable processor to alter its hardware compliment is typically accomplished through the use of some form of field programmable gate array ("FPGA")* such as those produced by Altera Corporation, Xilinx, Inc., Lucent Technologies, Inc. and others.
>
> In practice however, the application space over which such reconfigurable processors[] (as well as hybrids combining both microprocessors and FPGAs) can be practically employed is limited by several factors.
>
> Firstly, since FPGAs are less dense than microprocessors in terms of gate count, those packaged FPGAs having sufficient gates and pins to be employed as a general purpose reconfigurable processor ("GPRP"), are of necessity very large devices. This size factor alone may essentially prohibit their use in many portable applications.

Id. at 1:19–46 (emphasis added); *see also id*. at 2:12–21 ("create a particularly advantageous form of hybrid, reconfigurable processor module that overcomes the limitations of present discrete, integrated circuit device implementations of GPRP systems").

The patentee thus distinguished between "commodity microprocessors" and reconfigurable processors, and reconfigurable processors can merely "use" an FPGA. *Id*. at 1:19–35. Based on all of the foregoing, Defendants' reliance on *Alloc* for the proposition that "the very character of the invention requires the limitation be a part of every embodiment" is unpersuasive. *Alloc*, 342 F.3d at 1370. Defendants' reliance on *UltimatePointer* is likewise unavailing. *See UltimatePointer L.L.C. v. Nintendo Co.*, 816 F.3d 816, 823 (Fed. Cir. 2016) (construing "handheld device" to mean

"handheld direct pointing device" based on the title including "direct pointing," the specification disparaging indirect pointing, and the specification repeatedly emphasizing that the invention is directed to "direct pointing"; "The written description also emphasizes how direct pointing is superior to indirect pointing.").

Defendants cite statements by Plaintiff in IPR proceedings that "[t]he innovations in the '035 Patent relate to a new type of IC called a 'stacked die hybrid[']('SDH') processor, which facilitates the fabrication of a compact processor module having increased data speeds and processing efficiency," and "[t]he '035 Patent is directed to a particular type of SDH processor that includes a 'programmable array' on a first integrated circuit die." Dkt. No. 91, Ex. E, IPR 2020-01020 ('035 Patent), Sept. 4, 2020 Patent Owner's Preliminary Response at 1–2. Defendants fail to show that these statements, which appear in the "Introduction" section of the cited document, warrant limiting the meaning of "programmable array" in the '035 Patent as a whole. *See id*.

Defendants also argue that a "programmable array" must include a processor because the claimed invention requires a processor in order to be effective, and "certain claims require only 'programmable array' and 'memory.'" Dkt. No. 91 at 18. Yet, these claims also recite other limitations, such as regarding "contact points" that "traverse said die elements," which are discussed in the specification as being an improvement over prior techniques. *See* '035 Patent at Cls. 1 & 4. The opinion of Defendants' expert that "without the construction of the term 'programmable array' as proposed by Defendants, the claims of the patents-in-suit do not capture the purported invention disclosed in the patents-in-suit," is unpersuasive. Dkt. No. 91, Ex. A, Oct. 13, 2020 Liu Decl. at ¶ 53.

Finally, at the November 10, 2020 hearing, Plaintiff reiterated its argument that a "programmable array" could be memory, and Plaintiff emphasized disclosure of "memory array 40" and "array of logic cells 54":

> With reference additionally now to FIG. 2, a more detailed, simplified functional block diagram of the multi-adaptive processing element 14 illustrated in the preceding figure is shown. The multi-adaptive processing element 14 comprises, in pertinent part, a user logic block 32, which may comprise an FPGA together with its associated configuration ROM 34. A MAP control block 36 and associated direct memory access ("DMA") engine 38 as well as an on-board *memory array 40* is coupled to the user logic block 32 as well as the system bus 18.
>
> With reference additionally now to FIG. 3, a functional block diagram of a representative configuration data bus 50 is shown comprising a number of SRAM cells distributed throughout an FPGA comprising the user logic block 32 of the preceding figure. In a conventional implementation, the configuration information that programs the functionality of the chip is held in SRAM cells distributed throughout the FPGA as shown. Configuration data is loaded through a configuration data port 52 in a byte serial fashion and must configure the cells sequentially progressing through the entire *array of logic cells 54 and associated configuration memory 56*. It is the loading of this data through a relatively narrow, for example, 8 bit port that results in the long reconfiguration times.

'226 Patent at 3:53–4:9 (emphasis added).

This disclosure, however, does not associate the term "programmable array"—or even just the word "programmable"—with the disclosed "memory array" or the array of logic cells and associated memory. *See id.*

At the November 10, 2020 hearing, the Court asked counsel how the parties would respond to interpreting "programmable array" as referring to an array of functional elements configurable to create functional units. Plaintiff responded that to the extent this interpretation would exclude memory, such an interpretation would be inconsistent with disclosures in the specification regarding memory (discussed above). Defendants responded by maintaining their proposed construction but also, if the Court rejected Defendants' main proposed construction, Defendants

alternatively proposed: "array of reconfigurable functional elements configured to create functional units in hardware."

Based on the foregoing analysis, Plaintiff fails to demonstrate that a memory array can meet a claim limitation that recites a "programmable array." Plaintiff acknowledged at the November 10, 2020 hearing that the term "programmable array" includes FPGAs, and as noted above, the specification distinguishes between FPGA dies and "memory" dies. *See id*. at 4:14–24 & Fig. 4. Indeed, Plaintiff's recent arguments in IPR proceedings are consistent with this distinction:

> [T]he '035 Patent discloses stacking a thinned microprocessor die element, a *memory* die element, and a *programmable array (e.g. an FPGA)* and interconnecting the die elements using contacts that traverse the thickness of each die rather than being routed around the periphery of the stacked die elements.

Dkt. No. 91, Ex. E, IPR 2020-01020 ('035 Patent), Sept. 4, 2020 Patent Owner's Preliminary Response at 9 (emphasis added).

The Court therefore hereby expressly rejects Plaintiff's argument that memory can constitute a "programmable array." Finally, the Court adopts Defendants' proposal of "in hardware" as consistent with the intrinsic evidence. *See, e.g.,* '226 Patent at 1:19–46 (reproduced above).

Based on all of the foregoing, the Court hereby construes:

- **"programmable array"** to mean **"array of functional elements configurable to create functional units in hardware."**

D. "stacked with and electrically coupled to"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
No construction necessary – Plain and ordinary meaning which is adjacently placed and connected by electrical signals[11]	"directly connecting bare die elements placed on top of one another without intermediary packaging"

Dkt. No. 58 at 20; Dkt. No. 91 at 21; Dkt. No. 97 at 7; *see* Dkt. No. 79 at 21; *see also* Dkt. No. 104, Ex. A at 3. The parties submit that this term appears in Claims 13 and 22 of the '226 Patent, Claims 1, 4, 5, 8, and 10 of the '951 Patent, and Claims 1, 5, 9, 13, 17, and 25 of the '035 Patent. Dkt. No. 58 at 20; Dkt. No. 104, Ex. A at 3.

Shortly before the start of the November 10, 2020 hearing, the Court provided the parties with the following preliminary construction: "placed on top of one another in a stack with (without any packaging in between the die elements of the stack) and electrically connected to."

(1) The Parties' Positions

Plaintiff argues that "[t]his term means exactly what it states—the components are stacked (e.g. placed adjacent to each other), and connected by electrical signals." Dkt. No. 79 at 22. Plaintiff submits that "[t]he specification discloses that 'stacked' is meant to refer to placing different components in a manner that they can be considered a single functional block, but does not otherwise require a specific configuration." *Id*. (citing '035 Patent at 2:44–46 & '951 Patent at 2:53–55). Plaintiff also argues that "the patentee never acted as a lexicographer by defining this term and did not disclaim the scope of this term during prosecution." Dkt. No. 79 at 22.[12]

[11] Plaintiff previously proposed: "Plain and ordinary meaning." Dkt. No. 58 at 20; Dkt. No. 79 at 21.

[12] Plaintiff also cites the opinion of one of Defendants' experts in an IPR proceeding, which Plaintiff characterizes as an opinion that this term should be given its plain and ordinary meaning (Dkt. No. 79 at 22–23), but the cited opinion merely explains the position of Defendants' expert that no construction is necessary as to the non-means terms because: "[I]t is my opinion that for purposes of this proceeding, except for the 'means' terms, no other terms need be construed to

Defendants respond:

> Samsung's proposed construction relies on direct evidence from the patents' specifications and a POSITA's basic understanding as to the meanings of "stacked" and "electrically coupled to." Arbor's alleged "plain meaning" construction is anything but because it ignores the meaning of the claims, seeks to capture the very types of structures that the specification disparages, and again contradicts what Arbor recently told the Patent Office.

Dkt. No. 91 at 21. Defendants argue that "[b]ecause the plain meaning, the claims, and the specification, all require 'directly connecting bare die elements placed on top of one another without intermediary packaging,' it is not surprising that the patents distinguished and disparaged other techniques." *Id*. at 22; *see also id*. at 22–24. Likewise, Defendants cite "the specifications' disparagement of structures where the dies are not placed one on top of another." *Id*. at 26.

Plaintiff replies that this term "is readily understood by those in the art." Dkt. No. 97 at 7. Plaintiff urges that whereas "Arbor's use of the transitional phrase 'comprising' makes the claim 'open ended,' in that it requires all named elements to be present but does not exclude additional elements from also being present," Defendants' proposal of "without intermediary packaging" is a "negative limitation" that "improperly removes the scope of the transitional phrase 'comprising' from the claims." *Id*. Plaintiff argues that "as long as the accused products contain each of the claim elements, it is inconsequential whether they contain additional elements, such as intermediary packing." *Id*.

At the November 10, 2020 hearing, Defendants agreed with the Court's preliminary construction. Plaintiff argued that this term refers to orienting dies so as to permit electrical connections without using the periphery of the surface of a die, thereby allowing for elimination

---

resolve the prior art issues presented in this Petition. This is because, as detailed in Section X, each of the prior art grounds teaches, in relevant part, the exact same combination of features found in the only embodiment of the '226 Patent." Dkt. No. 79, Ex. 7, May 29, 2020 Shanfield Decl. at ¶ 53.

of wire bonds. Defendants argue that when the patents-in-suit refer to packaging, it is the *stack* that is packaged, not the individual dies.[13]

(2) Analysis

Claim 13 of the '226 Patent recites (emphasis added):

> 13. A processor module comprising:
> at least a first integrated circuit die element including a programmable array;
> at least a second integrated circuit die element including a processor *stacked with and electrically coupled to* said programmable array of said first integrated circuit die element;
> at least a third integrated circuit die element including a memory *stacked with and electrically coupled* to said programmable array and said processor of said first and second integrated circuit die elements respectively; and
> means for reconfiguring the programmable array within one clock cycle.

As to the phrase "coupled to," the specification discloses the following as to Figure 4:

> [T]he module 60 comprises a die package 62 to which is *coupled* a microprocessor die 64, memory die 66 and FPGA die 68, all of which have a number of corresponding contact points, or holes[] 70[,] formed throughout the area of the package 62 and various die 64, 66 and 68.

'226 Patent at 4:15–20 (emphasis added). The specification also refers to components being "couple[d]" to one another when discussing prior art, which weighs against construing "coupled to" as having a special, narrow meaning in the claimed invention. *See* '226 Patent at 3:47–50.

As to the term "stacked with," the Summary of the Invention refers to "stacking" multiple die elements to create a "block":

> Particularly disclosed herein is a processor module with reconfigurable capability constructed by *stacking* and interconnecting bare die elements. In a particular embodiment disclosed herein, a processor module with reconfigurable capability

[13] At the November 10, 2020 hearing, Defendants also presented portions of a rough transcript of the November 8, 2020 deposition of one of the named inventors. *See* Dkt. No. 122-1 at 105 (Defendants' presentation slides); *see also* Dkt. No. 116-1 (transcript).) Such testimony is of little, if any, relevance in these claim construction proceedings. *See Howmedica*, 540 F.3d at 1346–47 (noting that inventor testimony is "limited by the fact that an inventor understands the invention but may not understand the claims, which are typically drafted by the attorney prosecuting the patent application").

> may be constructed by *stacking* thinned die elements and interconnecting the same utilizing contacts that traverse the thickness of the die. As disclosed, such a processor module may comprise a microprocessor, memory and FPGA die *stacked* into a single block.

'226 Patent at 2:41–49 (emphasis added); '951 Patent at 2:53–55 (same); '035 Patent at 2:44–46 (same); *see also* '226 Patent at 1:11–18 ("the present invention relates to an extremely compact reconfigurable processor module comprising hybrid stacked integrated circuit ('IC') die elements").

The specification also refers to connections "routed up and down the stack," which implies that "stacked" elements are positioned one on top of another:

> It should be noted that although a single FPGA die 68 has been illustrated, two or more FPGA die 68 may be included in the reconfigurable module 60. Through the use of the through-die area array contacts 70, inter-cell connections currently limited to two dimensions of a single die, may be *routed up and down the stack* in three dimensions. This is not known to be possible with any other currently available stacking techniques since they all require the stacking contacts to be located on the periphery of the die.

Id. at 5:16–24 (emphasis added). This disclosure is thus consistent with Defendants' proposal of "on top of one another."

Further, the continuation-in-part '951 Patent discloses an embodiment in which one element can be "stacked on top of" another element:

> As an example, it is desired to have a Field Program[m]able Gate Array (FPGA) function *stacked on top of* and interconnected to a microprocessor functional element.

'951 Patent at 6:51–53 (emphasis added). Although this disclosure expressly refers to an example, this example is consistent with Defendants' proposal that "stacked" in this context refers to elements being placed on top of one another. *See id*.; *see also id*. at Fig. 9 (illustrating layers on top of one another).

The opinion of Plaintiff's expert, that "the components are stacked (e.g. placed one next to each other) *in any orientation*" is unpersuasive. Dkt. No. 80-1, Darveaux Decl. at ¶ 28 (emphasis modified); *see also id.* at ¶¶ 28–29. This interpretation by Plaintiff's expert lacks support in the specification and is inconsistent with the above-discussed disclosures. Further, Defendants submit extrinsic evidence to the contrary. In particular, Defendants cite a general-purpose dictionary that defines "stacked" as "having sections that are arranged vertically." Dkt. No. 91, Ex. I, *The New Oxford American Dictionary* 1657 (2001). Defendants also cite a general-purpose dictionary that defines "stack" as "a pile of things arranged *on top of one another*." Dkt. No. 91, Ex. H, *Cambridge Dictionary of American English* 841 (2000). Although extrinsic evidence is of limited weight, *see Phillips*, 415 F.3d at 1317–18, these dictionary definitions tend to reinforce the meaning of "stacked" that is evident from the specification as discussed above.

As to Defendants' proposal of "without intermediary packaging," the above-reproduced disclosure regarding "through-die area array contacts" is consistent with Defendants' suggestion of requiring what Defendants referred to at the November 10, 2020 hearing as "die-on-die" contact. *See* '226 Patent at 5:16–24. Further, the patent distinguishes other arrangements, such as stacking pre-packaged integrated circuits, collocating integrated circuits on a planar substrate (which might be referred to as a "side-by-side arrangement"), and including multiple integrated circuits within a single die:

> The disclosed technique for die interconnection used in forming the module of the present invention is *superior* to other available alternatives for several reasons. First, while it would be possible to *stack pre-packaged components* instead, the I/O connectivity between such parts would be much lower and limited to the parts' periphery, thereby obviating several of the advantages of the stacked die system disclosed. *Collocating multiple die on a planar substrate* is another possible technique, but that too suffers from limited I/O connectivity and again does not allow for area connections between parts. Another option would be to *fabricate a single die containing microprocessor, memory and FPGA*. Such a die could use metalization layers to interconnect the three functions and achieve much of the

> benefits of die stacking. However such a die would be extremely large resulting in a much lower production yield than the three separate die used in a *stacked configuration*. In addition, stacking allows for a ready mix of technology families on different die as well as offering a mix of processor and FPGA numbers and types. Attempting to effectuate this with a single large die would require differing mask sets for each combination, which would be very costly to implement.

Id. at 5:35–56 (emphasis added). These disparaged arrangements, such as stacking dies that each have their own packaging, should be excluded from the Court's construction. *See Poly-Am., L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016) ("an inventor may disavow claims lacking a particular feature when the specification distinguishes or disparages prior art based on the absence of that feature").

Defendants also cite statements by Plaintiff in IPR proceedings that "[t]he innovations in the '226 Patent relate to a new type of IC called a 'stacked die hybrid ('SDH') processor" and "[t]he SDH processor uses a wide number of *direct connections* between adjacent semiconductor dies." Dkt. No. 91, Ex. B, IPR2020-01022 ('226 Patent), Sept. 4, 2020 Patent Owner's Preliminary Response at 1–2 (emphasis added); *see also id*., Ex. E at 1–2; *id*., Ex. F, at 1–2. Although these statements do not amount to a lexicography, these statements are consistent with Defendants' proposal of requiring dies to be together within the same package, which is further supported by the specification disclosure reproduced above.

On balance, the above-discussed evidence supports Defendants' arguments that dies that are "stacked with" one another have so-called "die-on-die" contact with one another, and this can be given effect by referring to dies being within the same package. *See also* '226 Patent at 5:8–10 (referring to testing "*chips in the stack of the die package 62* during manufacture and prior to the completion of the *module packaging*") (emphasis added).

Finally, although Defendants' proposal of "bare" is based on disclosure in the Summary of the Invention, *see* '226 Patent at 2:41–43 ("stacking and interconnecting bare die elements"), and

although Defendants' proposal of "directly connecting" is consistent with Plaintiff's above-quoted statements in IPR proceedings, Dkt. No. 91, Ex. B, IPR2020-01022 ('226 Patent), Sept. 4, 2020 Patent Owner's Preliminary Response at 1–2, including "bare" and "directly connecting" in the construction of the disputed term would be unnecessary and potentially confusing in a construction that requires the recited dies to be within the same package.

The Court therefore hereby construes:

- **"stacked with and electrically coupled to"** to mean **"placed on top of one another in a stack, within the same package, and electrically connected to."**

E. "contact points distributed throughout the surfaces of said die elements" and "contact points distributed throughout the surfaces of said functional elements"

"contact points distributed throughout the surfaces of said die elements" ('226 Patent, Claims 19 and 28) ('035 Patent, Claims 1, 9, and 17)	
Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
No construction necessary – Plain and ordinary meaning which is contact points distributed on areas of the die elements surfaces[14]	"contact points distributed in every part of the die element surfaces rather than just around their periphery or just in the center"
"contact points distributed throughout the surfaces of said functional elements" ('951 Patent, Claims 1 and 15)	
Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
No construction necessary – Plain and ordinary meaning which is contact points distributed on areas of the functional elements surfaces[15]	"contact points distributed in every part of the functional element surfaces rather than just around their periphery or just in the center"

[14] Plaintiff previously proposed: "Plain and ordinary meaning." Dkt. No. 58 at 23; Dkt. No. 79 at 24.

[15] Plaintiff previously proposed: "Plain and ordinary meaning." Dkt. No. 58 at 25; Dkt. No. 79 at 24.

Dkt. No. 58 at 23 & 25; Dkt. No. 91 at 26; Dkt. No. 97 at 8; *see* Dkt. No. 79 at 24; *see also* Dkt. No. 104, Ex. A at 4.

Shortly before the start of the November 10, 2020 hearing, the Court provided the parties with the following preliminary constructions:

Term	Preliminary Construction
"contact points distributed throughout the surfaces of said die elements" ('226 Patent, Claims 19 and 28) ('035 Patent, Claims 1, 9, and 17)	"contact points distributed throughout the surfaces of said die elements rather than only around the peripheries of the surfaces"
"contact points distributed throughout the surfaces of said functional elements" ('951 Patent, Claims 1 and 15)	"contact points distributed throughout the surfaces of said functional elements rather than only around the peripheries of the surfaces"

(1) The Parties' Positions

Plaintiff argues that "these claim elements are straightforward – they simply mean that there are points of contact throughout the surface of the different die elements, as recited in the claims." Dkt. No. 79 at 24. Plaintiff argues that no lexicography or disavowal supports Defendants' proposals, and "Samsung's proposal only adds ambiguity because there is no description of what is meant by 'in every part of the die element' or in 'every part of the functional element surfaces.'" *Id*. at 25.[16]

[16] Plaintiff also cites the opinion of one of Defendants' experts in an IPR proceeding, which Plaintiff characterizes as an opinion that this term should be given its plain and ordinary meaning (Dkt. No. 79 at 26), but the cited opinion merely explains the position of Defendants' expert that no construction is necessary as to the non-means terms because: "[I]t is my opinion that for purposes of this proceeding, except for the 'means' terms, no other terms need be construed to resolve the prior art issues presented in this Petition. This is because, as detailed in Section X, each of the prior art grounds teaches, in relevant part, the exact same combination of features

Defendants respond that the patents-in-suit "distinguish distributing contacts 'throughout' the die surfaces from confining the contacts to a particular location," and "contact points 'throughout' is integral to the 'one clock cycle' limitation."

Plaintiff replies that "[b]ecause Samsung's construction adds limitation without evidence demonstrating a clear intent to limit the claim term, the terms should be given its plain and ordinary meaning." Dkt. No. 97 at 9. Plaintiff also argues:

> [T]he specification uses the term "throughout" in a manner that is contradictory to Samsung's proposed construction because it shows that to be "throughout" does not require distribution in "ever[y] part of the die element surfaces." Specifically, its states that [*sic*, refers to] "static random access memory ('SRAM') cells distributed throughout the FPGA." However, static random access memory would could [*sic*] only be part of an FPGA, and would not be used for "every part" of the die for the FPGA. Ex. 1 [('226 Patent)], 3:25–28.

Id.

At the November 10, 2020 hearing, the parties presented no oral argument and submitted these disputed terms on the briefing.

(2) Analysis

Claim 1 of the '951 Patent, for example, recites (emphasis added):

> 1. A processor module comprising:
>
> at least a first integrated circuit functional element including a programmable array that is programmable as a processing element; and
>
> at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element wherein said first and second integrated circuit functional elements are electrically coupled by a number of *contact points distributed throughout the surfaces of said functional elements* and wherein said second integrated circuit includes a memory array functional to accelerate external memory references to the processing element.

The Summary of the Invention states:

---

found in the only embodiment of the '226 Patent." Dkt. No. 79, Ex. 7, May 29, 2020 Shanfield Decl. at ¶ 53.

> [S]ince these differing die do not require wire bonding to interconnect, it is now also possible to place interconnect pads *throughout the total area* of the various die *rather than just around their periphery*. This then allows for many more connections between the die than could be achieved with any other known technique.

'226 Patent at 2:34–40 (emphasis added). The specification further discusses contacts formed throughout areas:

> In this particular implementation, the module 60 comprises a die package 62 to which is coupled a microprocessor die 64, memory die 66 and FPGA die 68, all of which have a number of corresponding contact points, or holes[] 70[,] formed *throughout the area* of the package 62 and various die 64, 66 and 68.
>
> * * *
>
> [W]hile it would be possible to stack pre-packaged components instead, the I/O connectivity between such parts would be much lower and limited to the parts' *periphery*, thereby obviating several of the advantages of the stacked die system disclosed.

Id. at 4:15–19 & 5:35–45 (emphasis added); '951 Patent at 4:66–5:4; '035 Patent at 4:11–16; *see also* '226 Patent at 4:34–44.

These disclosures use "throughout" in contrast to the "periphery." Further, although "patent coverage is not necessarily limited to inventions that look like the ones in the figures," *MBO Labs., Inc. v. Becton, Dickinson & Co.*, 474 F.3d 1323, 1333 (Fed. Cir. 2007), Figure 4 of the patents-in-suit reinforces that the above-reproduced disclosure is consistent with interpreting "throughout" as contrasting with the connections being placed only at the peripheries of elements. Plaintiff's recent statements in IPR proceedings are consistent with this understanding. *See* Dkt. No. 91, Ex. B, IPR 2020-01022 ('226 Patent), Sept. 20, 2020 Patent Owner Preliminary Response at 2 ("These die-area contacts distinguish the '226 Patent from earlier approaches, such as that disclosed in the Cooke reference, where stacked dies are electrically connected via metallization contacts at the edges of the die.").

This contrast should be reflected in the Court's construction. The opinions of Plaintiff's expert to the contrary are unpersuasive. *See* Dkt. No. 80-1, Sept. 29, 2020 Darveaux Decl. at ¶¶ 30–31.

Defendants' proposals of "in every part" and "rather than . . . just in the center," however, are unclear and lack sufficient support in the intrinsic evidence. Defendants cite general-purpose dictionaries that define "throughout" as meaning "through the whole of; in every part of" and as meaning "in every part, or during the whole period of." Dkt. No. 91, Ex. J, *Webster's New World College Dictionary* 1493 (4th ed. 2001); *id*., Ex. H, *Cambridge Dictionary of American English* 908 (2000). These general-purpose dictionary definitions do not adequately support Defendants' proposal in the context of the patents-in-suit. *See Phillips*, 415 F.3d at 1321 ("heavy reliance on the dictionary divorced from the intrinsic evidence risks transforming the meaning of the claim term to the artisan into the meaning of the term in the abstract, out of its particular context, which is the specification"). The opinions of Defendants' expert in this regard do not compel otherwise. *See* Dkt. No. 91, Ex. A, Oct. 13, 2020 Liu Decl. at ¶¶ 78–82.[17]

The Court therefore hereby construes these disputed terms as set forth in the following chart:

[17] In its reply brief, Plaintiff cites the "Brief Description" of Figure 3, which uses the word "throughout": "FIG. 3 is a functional block diagram of a representative configuration data bus comprising a number of static random access memory ('SRAM') cells distributed *throughout* the FPGA comprising the user logic lock of FIG. 2." '226 Patent at 3:25–28 (emphasis added). Plaintiff argues that "static random access memory would could [*sic*] only be part of an FPGA, and would not be used for 'every part' of the die for the FPGA." Dkt. No. 97 at 9. On balance, Plaintiff fails to adequately support its argument in this regard, and in any event Plaintiff's argument does not alter the Court's analysis of these disputed terms.

Term	Construction
"contact points distributed throughout the surfaces of said die elements"	**"contact points distributed throughout the surfaces of said die elements rather than only around the peripheries of the surfaces"**
"contact points distributed throughout the surfaces of said functional elements"	**"contact points distributed throughout the surfaces of said functional elements rather than only around the peripheries of the surfaces"**

F. "a memory array functional to accelerate external memory references to the processing element," "wherein said memory array is functional to accelerate external memory references to the processing element," and "wherein said memory is functional to accelerate external memory references to said programmable array"

"a memory array functional to accelerate external memory references to the processing element" ('951 Patent, Claim 1)	
Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
Plain and ordinary meaning	Indefinite
"wherein said memory array is functional to accelerate external memory references to the processing element" ('951 Patent, Claim 5)	
Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
Plain and ordinary meaning	Indefinite
"wherein said memory is functional to accelerate external memory references to said programmable array" ('951 Patent, Claim 10)	
Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
Plain and ordinary meaning	Indefinite

Dkt. No. 58 at 28, 30–31 & 33; Dkt. No. 79 at 26; Dkt. No. 97 at 9; Dkt. No. 104, Ex. A at 4–5; *see also* Dkt. No. 91 at 30.

Shortly before the start of the November 10, 2020 hearing, the Court provided the parties with the following preliminary construction for these disputed terms: "Plain meaning."

(1) The Parties' Positions

Plaintiff argues that these terms are readily understandable to a person of ordinary skill in the art, and "the claim language is basically reciting that the memory array is used in the claims to speed up references to external memory by using the already recited memory array, for example, as an intermediary buffer." Dkt. No. 79 at 27. Plaintiff also submits that "[t]he specification teaches in several sections that the short interconnects to the memory die allows for accelerated external memory references, providing additional context for a POSITA to interpret the claims." *Id*. at 29. "Finally," Plaintiff argues, "the use of the word 'accelerate' does not render the claim indefinite because it has an ordinary meaning that can be applied with a reasonable level of certain[ty] by a POSITA," and "[t]he '951 Patent provides an objective boundary to a POSITA to understand that close proximity of interconnects to the memory die provide an accelerated external memory reference over the prior art system shown in Fig. 3." *Id*. at 29–30.

Defendants argue that "[t]he term 'accelerate' . . . refers to a comparison between two speeds without providing any basis for comparison," and "[t]he specification also does not provide an objective basis by which a POSITA could determine the scope of when the 'accelerate' limitations are met." Dkt. No. 91 at 28. Defendants argue that the relevant disclosures in the specification "do not define the scope of or provide a comparative baseline for 'accelerate.'" *Id*. at 29. For example, Defendants argue that "there are many factors and design considerations that would determine whether a configuration using short interconnects, like those found in through

silicon vias, would result in faster data sharing than a ball grid array configuration, for example." *Id*. at 29–30.[18]

Plaintiff replies that "[a] POSITA understands that these claim limitations require a memory array that is able to speed up, or make memory references faster, than otherwise be [*sic*] without the memory array." Dkt. No. 97 at 10. "For example," Plaintiff argues, "a POSITA would understand the claims as reciting that the memory array is used to speed up references to external memory by using the already recited memory array, for example, as an intermediary buffer." *Id*.

At the November 10, 2020 hearing, Defendants reiterated that the claims and the specification fail to explain what the acceleration is relative to, and Defendants submitted examples such as operating at a higher clock speed, being faster than other types of memory, or being faster than using no memory array at all. Defendants argued that the patent provides no context or guidance in this regard.

(2) Analysis

Claim 1 of the '951 Patent, for example, recites (emphasis added):

> 1. A processor module comprising:
>
> at least a first integrated circuit functional element including a programmable array that is programmable as a processing element; and
>
> at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements and wherein said second integrated circuit includes *a memory array functional to accelerate external memory references to the processing element*.

[18] Defendants also cite the Court's adoption of an agreed-upon construction of "accelerated data storage and retrieval" in *Realtime Data, LLC, v. Oracle America, Inc., et al.* as meaning "compressing and storing data in less time than data can be stored in uncompressed form; and retrieving and decompressing data in less time than data can be retrieved in uncompressed form" (Dkt. No. 91 at 28 (citing No. 6:16-CV-88, Dkt. No. 83 at 10 (E.D. Tex. Oct. 28, 2016)), but the Court's adoption of that agreed-upon construction in *Realtime* is of no persuasive weight as to the disputed terms in the present case.

In some cases, "[t]he hazy relationship between the claims and the written description fails to provide the clarity that the subjective claim language needs." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1372 (Fed. Cir. 2014). In the present case, however, Defendants do not show that "accelerate" is "subjective," *Id.* Furthermore, the specification describes accelerating external memory references:

> Also disclosed herein is a processor module with reconfigurable capability that may include, for example, a microprocessor, memory and FPGA die stacked into a single block for the purpose of *accelerating* the sharing of data between the microprocessor and FPGA. Such a processor module block configuration advantageously increases final assembly yield while concomitantly reducing final assembly cost.
>
> Further disclosed herein is an FPGA module that uses stacking techniques to combine it with a memory die for the purpose of *accelerating* FPGA reconfiguration. In a particular embodiment disclosed herein, the FPGA module may employ stacking techniques to combine it with a memory die for the purpose of *accelerating* external memory references as well as to expand its on chip block memory.
>
> * * *
>
> With reference additionally now to FIG. 5, a corresponding functional block diagram of the configuration cells 80 of the reconfigurable processor module 60 of the preceding figure is shown wherein the FPGA 70 may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel. As opposed to the conventional implementation of FIG. 3, a wide configuration data port 82 is included to update the various logic cells 84 through an associated configuration memory 86 and buffer cell 88. The buffer cells 88 are preferably a portion of the memory die 66 (FIG. 4). In this manner, they can be loaded while the FPGA 68 comprising the logic cells 84 are in operation. This then enables the FPGA 68 to be totally reconfigured in one clock cycle with all of it[s] configuration logic cells 84 updated in parallel. Other methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory ("RAM") than can be offered within the FPGA die 68 itself.
>
> In addition to these benefits, there is an added benefit of overall reduced power requirements and increased operational bandwidth. Because the various die 64, 66

> and 68 (FIG. 4) have *very short electrical paths* between them, the signal levels can be reduced while at the same time the interconnect clock *speeds* can be *increased*.

'951 Patent at 2:56–3:2 & 5:29–56; *see also id*. at Figs. 4 & 5; *see also* '951 Patent at Abstract ("The processor module disclosed allows for a significant *acceleration* in the sharing of data between the microprocessor and the FPGA element . . . .") (emphasis added).

The word "accelerated" does not give rise to indefiniteness because the relative speeds and the precise manner of acceleration are implementation-specific details. *See Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576 (Fed. Cir. 1986) (regarding a chair leg portion "so dimensioned as to be insertable through the space between the doorframe of an automobile and one of the seats thereof," finding that "[t]he patent law does not require that all possible lengths corresponding to the spaces in hundreds of different automobiles be listed in the patent, let alone that they be listed in the claims"); *see also Nautilus*, 134 S. Ct. at 2128 (citation and internal quotation marks omitted); *id*. at 2128 n.5 (citing *Eibel Process Co. v. Minn. & Ontario Paper Co.*, 261 U.S. 45, 58, 65-66 (1923) (Taft, J.), as "upholding as definite a patent for an improvement to a paper-making machine, which provided that a wire be placed at a 'high' or 'substantial elevation,' where 'readers . . . skilled in the art of paper making and versed in the use of the . . . machine' would have 'no difficulty . . . in determining . . . the substantial [elevation] needed' for the machine to operate as specified") (ellipses and square bracketed text are the Court's in *Nautilus*); *id*. at 2129 ("The definiteness requirement . . . mandates clarity, while recognizing that absolute precision is unattainable."); *Interval Licensing*, 766 F.3d at 1370 ("We do not understand the Supreme Court to have implied in *Nautilus* . . . that terms of degree are inherently indefinite.")

The opinions of Plaintiff's expert are also persuasive. *See* Dkt. No. 80-1, Sept. 29, 2020 Darveaux Decl. at ¶¶ 32–37. For example, Plaintiff's expert opines that "Figures 4 and 5 of the specification discloses a memory die 66 which is a memory array and a buffer cell which can be

part of the memory die with short interconnects, thus improving the speed of an intermediary buffer and access to memory in comparison to the prior art." *Id*. at ¶ 33.

The contrary opinions of Defendants' expert are unpersuasive. Dkt. No. 91, Ex. A, Oct. 13, 2020 Liu Decl. at ¶¶ 84–92. For example, Defendants' expert opines that data sharing between integrated circuit dies connected through surface area contacts, as disclosed in the specification, may or may not be faster than data sharing between integrated circuits connected through other means. *Id*. at ¶ 88. The disputed terms, however, expressly require acceleration. Defendants' expert also opines that a person of ordinary skill "would not know what baseline speed the claimed acceleration can be measured against and compared to," *id*. at ¶ 87, and "if not for the specific configuration disclosed in the specification, a POSITA would not know the boundaries of what it means to 'accelerate' data transfer for systems that do not include the claimed structure," *id*. at ¶¶ 87 & 91, but Defendants' own expert in IPR proceedings evidently understood the meaning of "accelerate" in this context, opining as to certain prior art references that although the limitation "is unclear because neither the claims nor the specification describes a baseline from which to measure the claimed acceleration," a "prior art combination discloses the same way to *accelerate* external memory references as is described in the '951 Patent specification." Dkt. No. 79, Ex. 9, May 29, 2020 Shanfield Decl. at ¶ 90 (emphasis added).

Finally, Defendants note the patent examiner's Reasons for Allowance, in which the examiner stated:

> The following is an examiner's statement of reasons for allowance: the best prior art of record, Lin, taken alone or in combination of other references, does not teach or fairly suggest an integrated circuit comprising, among other things, that wherein said memory array is functional to accelerate external memory references to said processing element, as set forth in the claims.

Dkt. No. 91, Ex. K, at 2 (ARBOR-SAM000218). Defendants conclude that the disputed terms were "instrumental" to the basis for allowance of the '951 Patent and, therefore, Plaintiff cannot argue that "simply satisfying the remaining portions of the claims is [] sufficient to satisfy the 'accelerate' terms." Dkt. No. 91 at 30. Plaintiff's argument in this regard, however, does not significantly affect the Court's analysis, so Defendants' counterargument is of no moment.

Based on all of the foregoing, Defendants fail to meet their burden to show indefiniteness. *See Sonix Tech. Co. v. Publ'ns Int'l, Ltd.*, 844 F.3d 1370, 1377 (Fed. Cir. 2017) ("Indefiniteness must be proven by clear and convincing evidence."). The disputed terms "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus*, 134 S. Ct. at 2129.

The Court therefore hereby expressly rejects Defendants' indefiniteness argument. Defendants do not present any alternative proposed construction. The Court accordingly hereby construes the following terms as having their **plain meaning**:

- **"a memory array functional to accelerate external memory references to the processing element,"**
- **"wherein said memory array is functional to accelerate external memory references to the processing element,"** and
- **"wherein said memory is functional to accelerate external memory references to said programmable array."**

V. CONCLUSION

The Court adopts the constructions set forth in this opinion for the disputed terms of the patents-in-suit. The parties are ordered that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court,

in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

SIGNED this 3rd day of December, 2020.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE